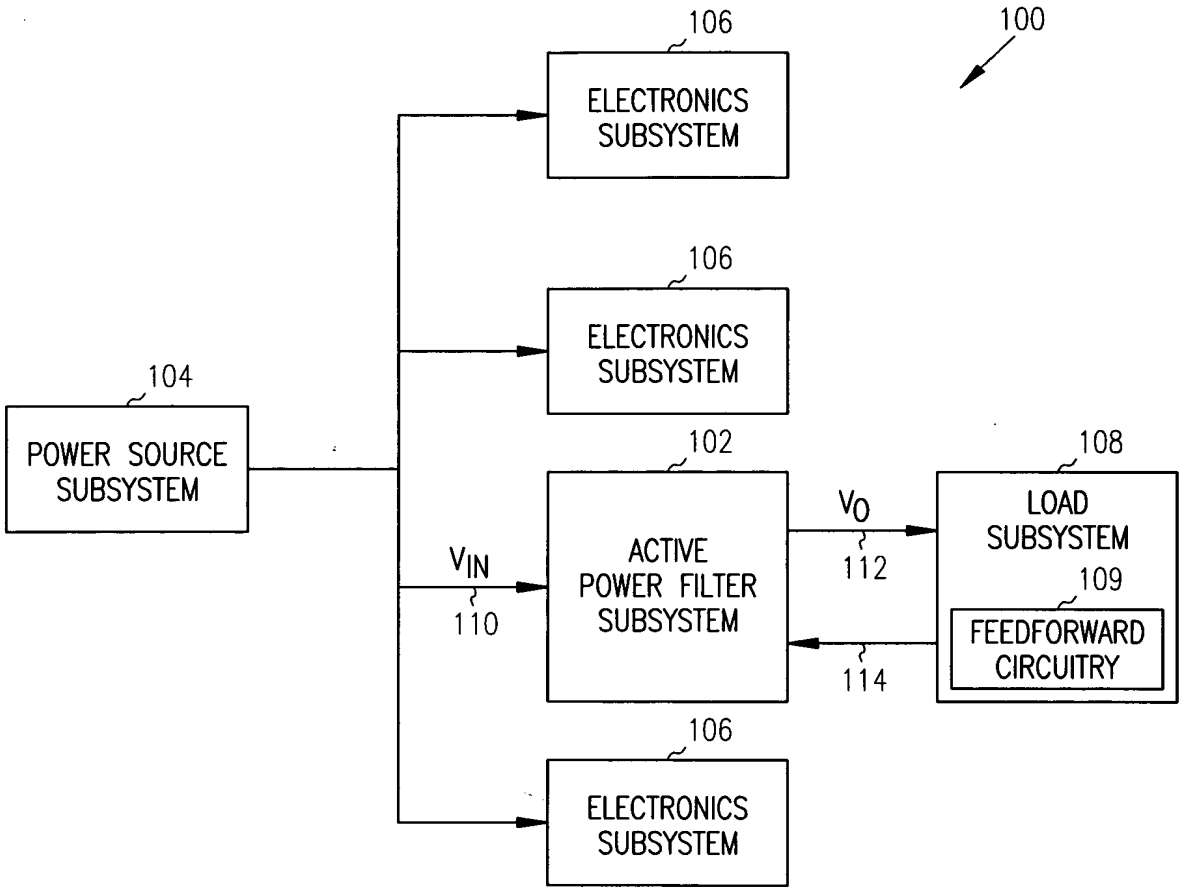
100
106
ELECTRONICS SUBSYSTEM
106
ELECTRONICS SUBSYSTEM
104
POWER SOURCE SUBSYSTEM
102
ACTIVE POWER FILTER SUBSYSTEM
$V_{IN}$
110
$V_O$
112
114
108
LOAD SUBSYSTEM
109
FEEDFORWARD CIRCUITRY
106
ELECTRONICS SUBSYSTEM

FIG. 1

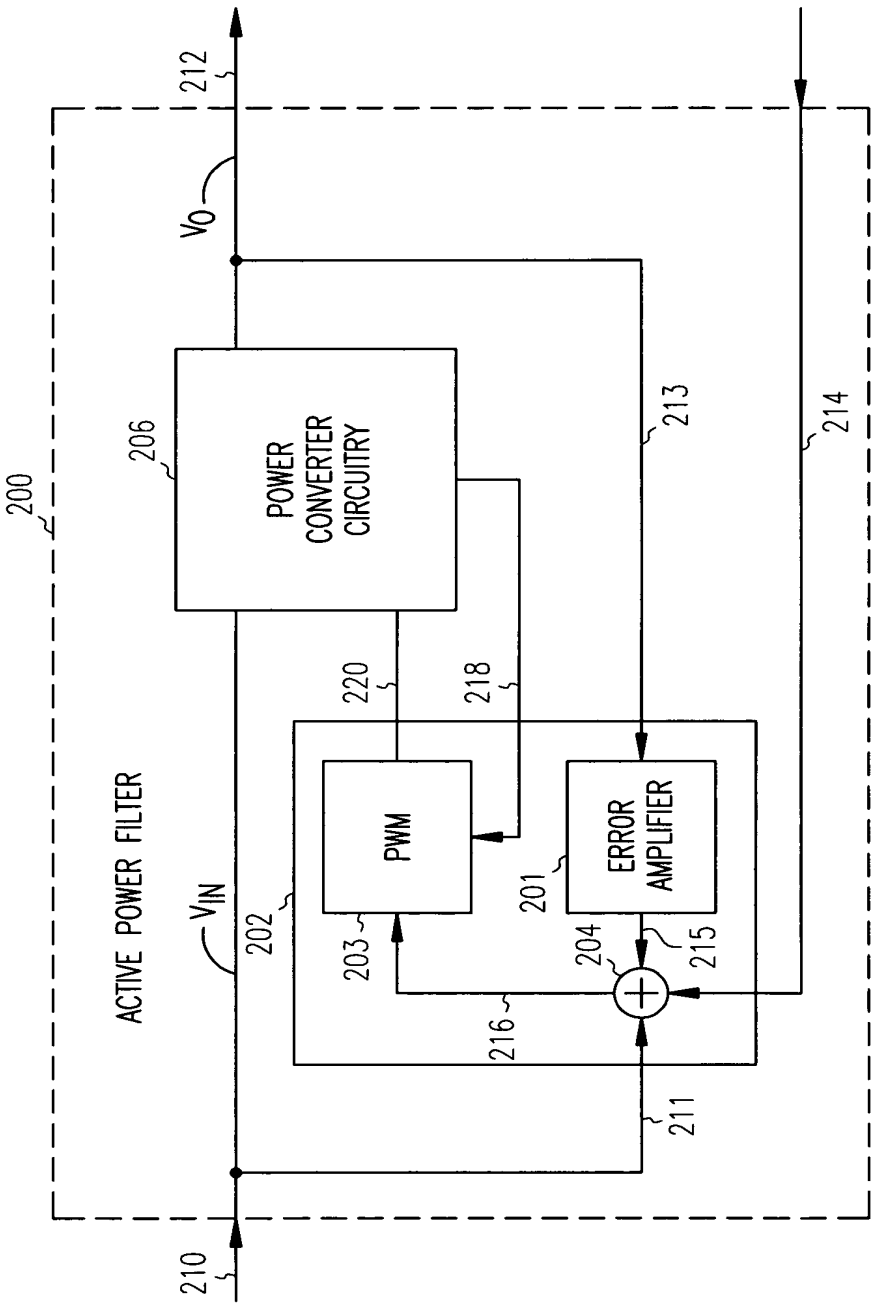
212
$V_O$
206
POWER CONVERTER CIRCUITRY
213
214
200
220
218
ACTIVE POWER FILTER
PWM
ERROR AMPLIFIER
$V_{IN}$
202
201
203
204
215
216
211
210

FIG. 2

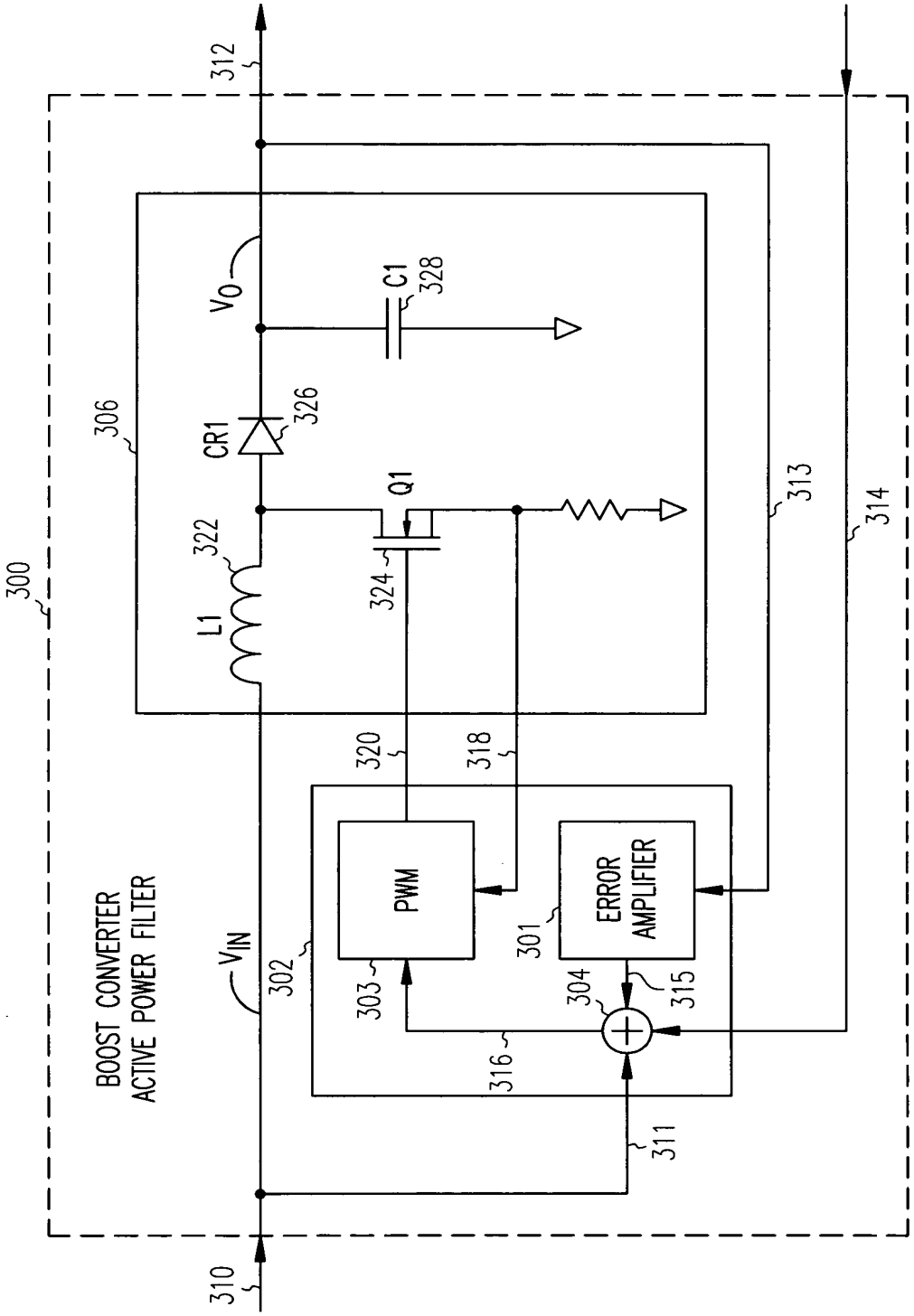
312
$V_O$
C1
328
306
CR1
326
Q1
313
314
322
300
324
L1
320
318
PWM
ERROR AMPLIFIER
301
BOOST CONVERTER ACTIVE POWER FILTER
$V_{IN}$
302
303
304
315
316
311
310

FIG. 3

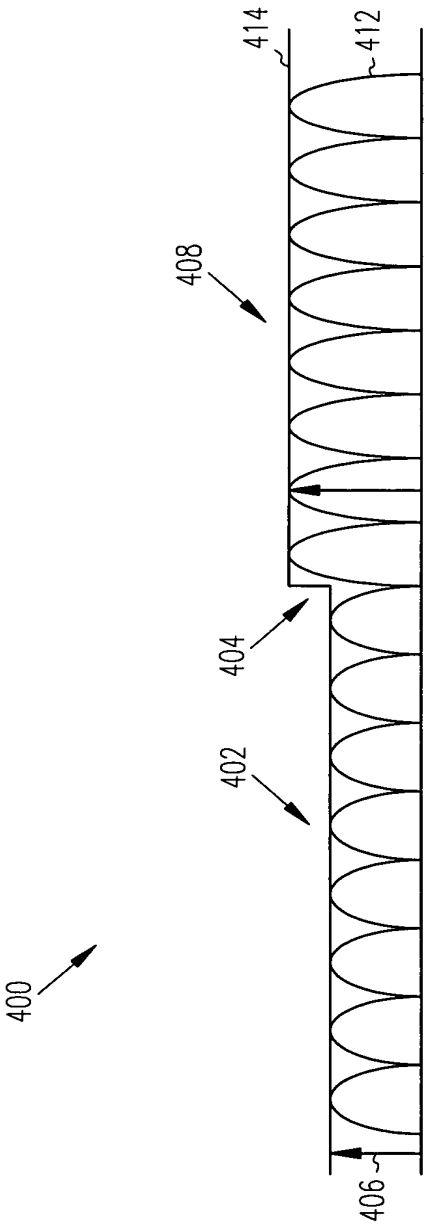


FIG. 4

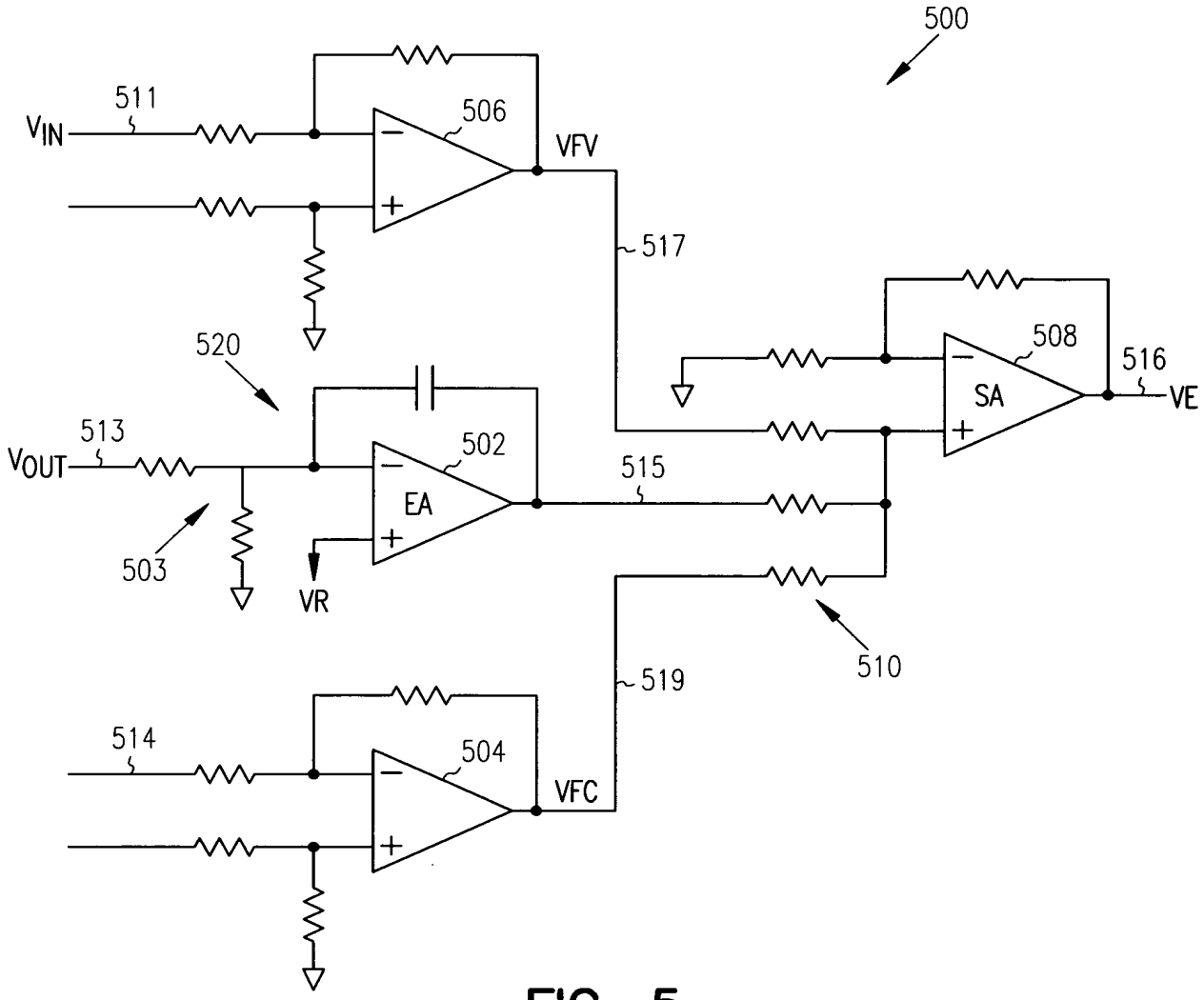
500
511
$V_{IN}$
506
VFV
517
520
508
516
SA
VE
513
$V_{OUT}$
502
EA
515
503
VR
510
519
514
504
VFC

FIG. 5

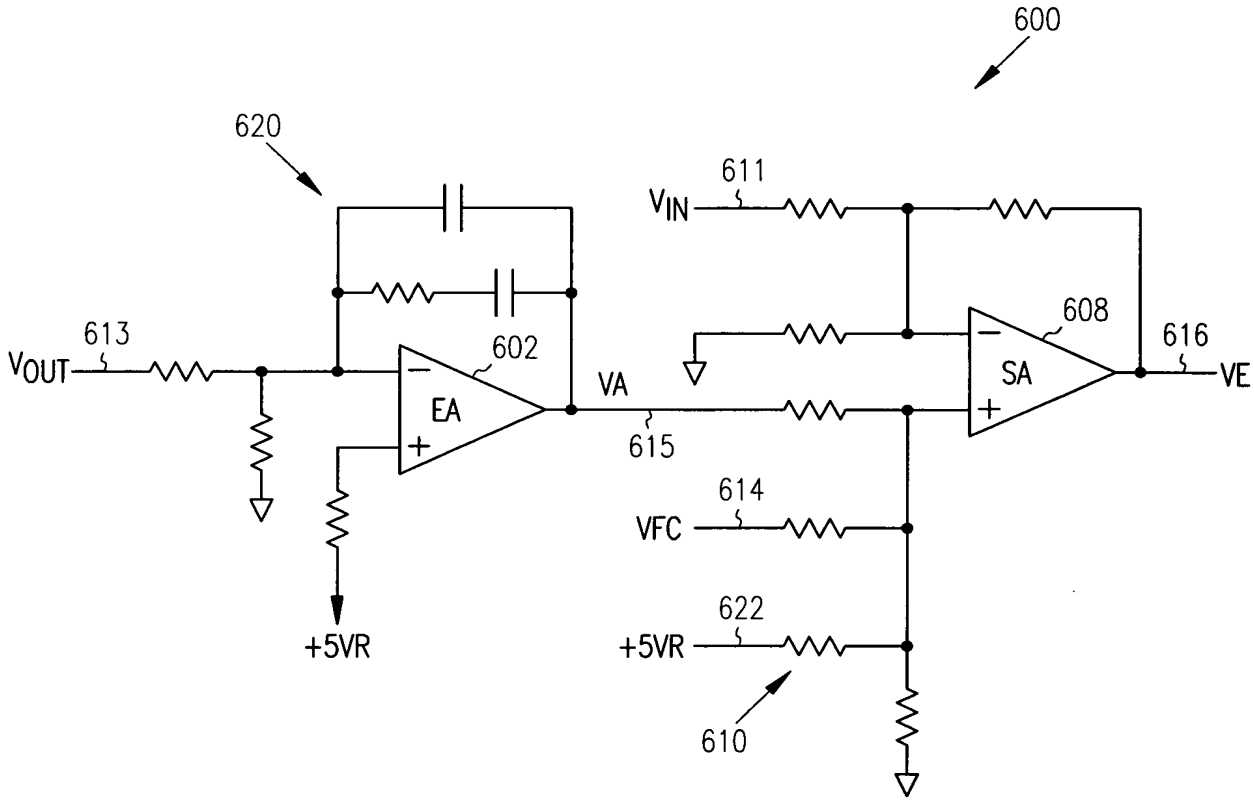
600
620
611
$V_{IN}$
613
$V_{OUT}$
602
EA
VA
615
608
SA
616
VE
614
VFC
622
+5VR
+5VR
610

FIG. 6

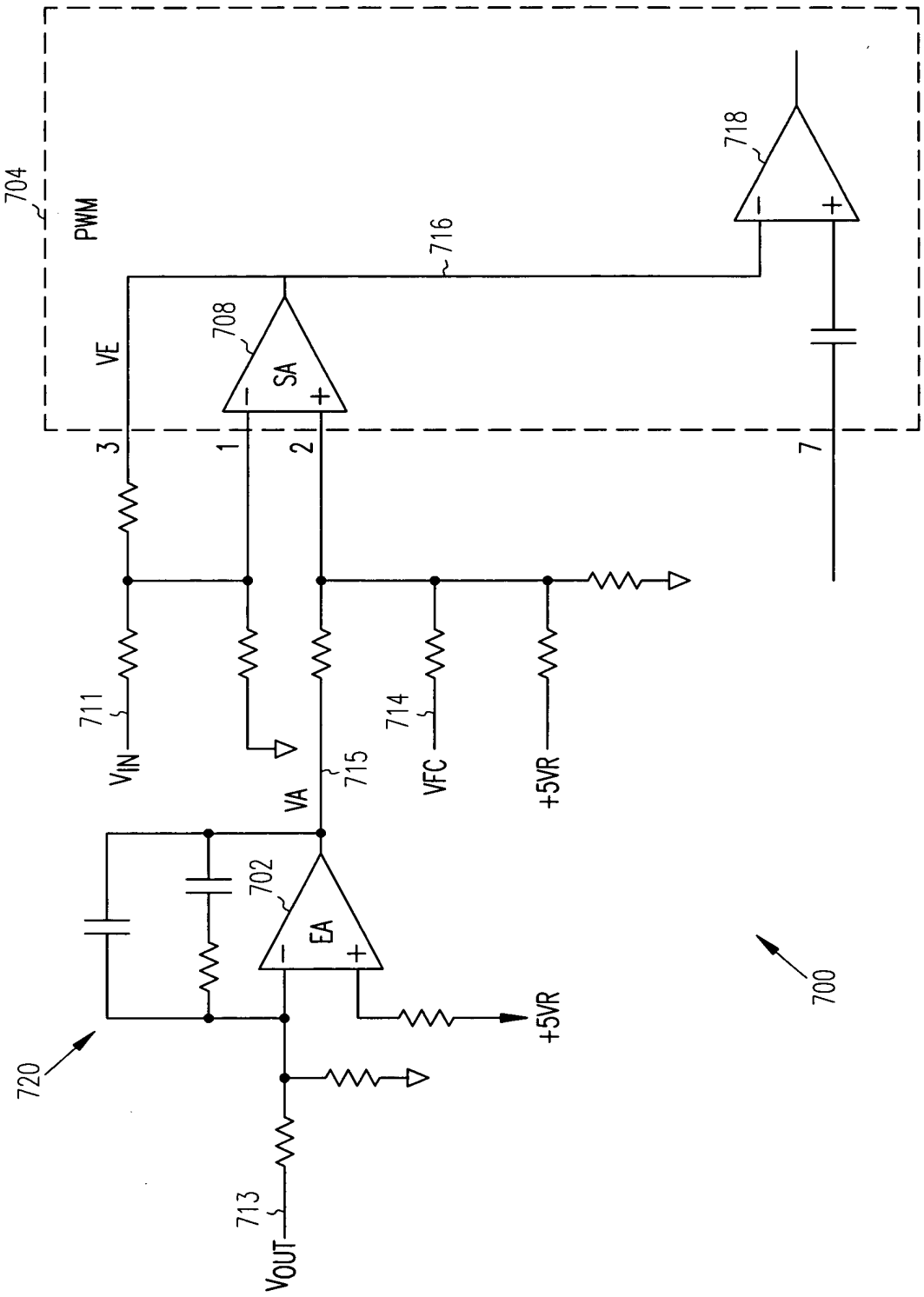
704
PWM
VE
3
708
SA
1
2
716
718
7
711
VIN
VA
715
714
VFC
+5VR
702
EA
+5VR
720
700
713
VOUT

FIG. 7

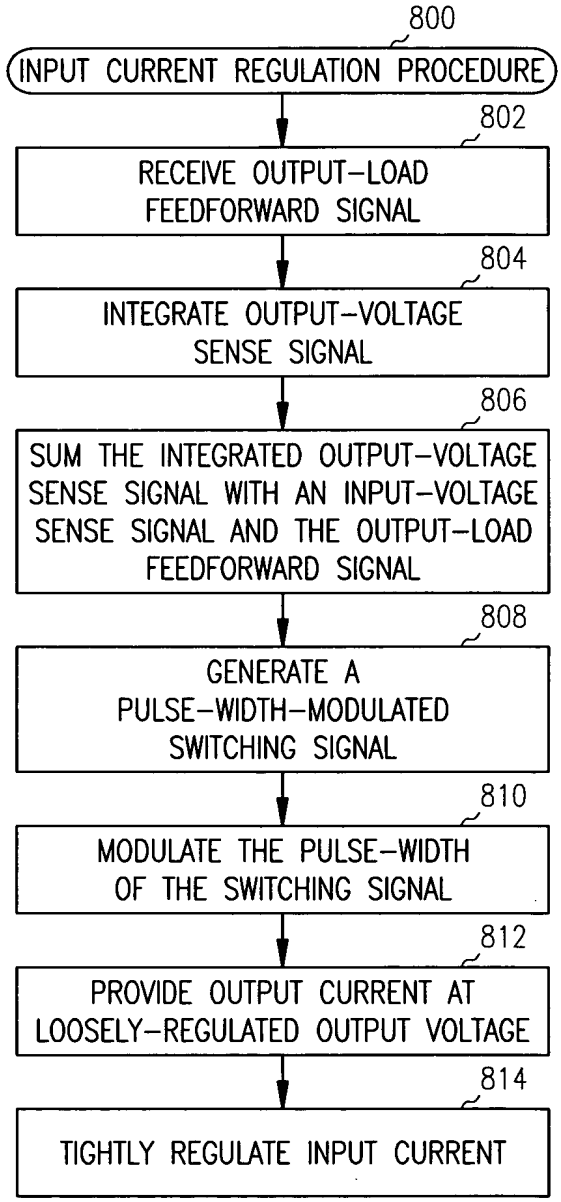
800
INPUT CURRENT REGULATION PROCEDURE
802
RECEIVE OUTPUT-LOAD FEEDFORWARD SIGNAL
804
INTEGRATE OUTPUT-VOLTAGE SENSE SIGNAL
806
SUM THE INTEGRATED OUTPUT-VOLTAGE SENSE SIGNAL WITH AN INPUT-VOLTAGE SENSE SIGNAL AND THE OUTPUT-LOAD FEEDFORWARD SIGNAL
808
GENERATE A PULSE-WIDTH-MODULATED SWITCHING SIGNAL
810
MODULATE THE PULSE-WIDTH OF THE SWITCHING SIGNAL
812
PROVIDE OUTPUT CURRENT AT LOOSELY-REGULATED OUTPUT VOLTAGE
814
TIGHTLY REGULATE INPUT CURRENT

FIG. 8